

Appl. No. 09/617,450
Am dt. dated October 1, 2004
Reply of Office Action of May 20, 2004

AMENDMENTS TO THE CLAIMS

Claims 1-12 were amended in the Preliminary Amendment filed July 17, 2000.

Claims 1-12 are currently pending. Please cancel claims 1-7 and 10-12 without prejudice or disclaimer in the subject matter and amend claim 8 as set forth in the following listing of the claims:

1-7 (canceled)

8. (currently amended) The method as claimed in claim 5, A method for modulating a basic clock signal for digital circuits, in which distances between adjacent switching edges are altered, the basic clock signal being conducted via a changing number of delay units for altering the distances between the adjacent switching edges, said method comprising the step of calibrating delay times of the delay units (D1-Dn), wherein the delay units (D1-Dn) each have a plurality of delay elements (10) which are controlled to impart zero delay or a non-zero value of delay to a clock signal individually or in groups of the ~~delay~~ elements; wherein the respective distance between two adjacent switching edges is derived from numbers of a random number

random number generator; and wherein the distance between two successive switching edges is derived as a function of the random number and a modulation factor.

9. (previously presented) The method as claimed in claim 8, further comprising the step of calculating the position of a switching edge (a_{i+1}) succeeding a switching edge (a_i) [is calculated] as follows:

$$a_{i+1} = (a_i + p - \frac{(N-1 - z_{i+1})K}{2}) \bmod p$$

where

p represents the number of delay steps per half-period,

N represents the number of possible switching edges,

K represents the modulation factor, and

z represents the random number.

10-12 cancelled